REMARKS

Claims 1 and 14 have been amended to be dependent from claim 10. Thus, claim 10 is generic to Species 1-5. Also claims 6-8, 14 and 17 have been amended for further clarity.

In the Office Action, it was indicated that the application contained claims directed to:

Species I, figures 1A-1H, Species II, figures 2A-2F; Species III, figures 3A-3M; Species IV, figures 5A-5H (formed prior to the source/drain region); Species V, figures 5A-5H (formed subsequent to the source/drain regions); Species VI, figures 6A-6J, and Species VII, figures 8A-8J. It was indicated that no claims were generic to any of the species of the invention as disclosed in the specification. It was therefore required that applicant identify the species for prosecution on the merits to which the claims shall be restricted.

Applicant hereby elects Species VI, Figures 5A-5H, wherein the resistor element is formed prior to the source/drain regions. It is submitted that claims 1-17 now read on the elected species for examination on the merits in this application.

Applicants reserve the right to file one or more divisional applications directed to the subject matter of the non-elected species.

Favorable consideration the subject application is respectfully requested.

In the event this paper is not timely filed, the undersigned hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this response.

Respectfully submitted,

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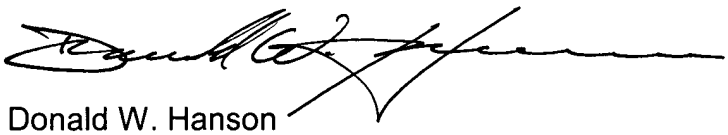

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MARKED UP VERSION OF AMENDMENTS TO CLAIMS AND SPECIFICATION

IN THE CLAIMS:

Amend the claims as follows:

1. (Amended) A method of manufacturing a semiconductor device according to claim 10, wherein~~, comprising the steps of:~~

~~(a) preparing a semiconductor substrate having first and second regions of a first conductivity type defined in a principal surface area of the semiconductor substrate;~~

said step (b) ~~forming~~ forms first and second gate electrodes in respective partial areas of said first and second regions;

said step (c) ~~by using the second gate electrodes as a mask, implanting~~ implants impurities of ~~a~~ the second conductivity type ~~opposite to said first conductivity type~~ into ~~each~~ a surface layer in said second ~~regions and thereafter executing a first activation process to form first impurity diffusion regions~~ region on both sides of said second gate electrode;

said step (d) ~~forming~~ forms first spacer films on side surfaces of said first and second gate electrodes; and

said step (e) ~~by using said first and second gate electrodes and said first spacer films as a mask, implanting~~ implants impurities of said second conductivity type into surface layers in said first and second regions ~~and thereafter executing a second activation process~~ to form second impurity diffusion regions~~;~~

~~(f) removing said first spacer films; and~~

~~(g) by using said first gate electrodes as a mask, implanting impurities of said second conductivity type into each surface layer in said first regions and thereafter executing a third activation process to form third impurity diffusion regions, wherein said third activation process is executed so that the gradient of an impurity concentration distribution in a p-n junction formed by said third impurity diffusion regions becomes steeper than the gradient of an impurity concentration distribution in a p-n junction formed by said first impurity diffusion regions formed by said first activation process~~.

6. (Amended) A method of manufacturing a semiconductor device according to claim 5, wherein said process (g) comprises a step of forming an absorption layer which improves an absorption efficiency of laser radiated to said semiconductor substrate, a step of implanting impurity ions of the second conductivity type into at least said first ~~regions~~ region by using said first gate ~~electrodes~~ electrode as a mask, and a step of executing a thermal treatment by said laser thermal process.

7. (Amended) A method of manufacturing a semiconductor device according to claim 1, wherein at least the first gate ~~electrodes are dummy gate electrodes~~ electrode is a dummy gate electrode, and the method further comprises, after said step (g), a step of forming an insulating film over said semiconductor substrate, said insulating film having etching characteristics different from material of said dummy gate electrode, and planarizing a surface of said insulating film to expose upper surfaces of said dummy gate ~~electrodes~~ electrode, a step of selectively removing said dummy gate ~~electrodes~~ electrode

selectively with respect to said insulating film, and a step of burying conductive material in ~~spaces~~ a space from which said dummy gate ~~electrodes were~~ electrode has been removed.

8. (Amended) A method of manufacturing a semiconductor device according to claim 1, wherein the ~~shortest~~ gate length ~~among~~ of said first gate ~~electrodes~~ electrode is shorter than the ~~shortest~~ gate length ~~among~~ of said second gate ~~electrodes~~ electrode.

10. (Amended) A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor substrate having first and second regions of a first conductivity type defined in a principal surface area of the semiconductor substrate;

(b) forming at least a first gate ~~electrodes~~ electrode in a partial area of the first region;

(c) implanting impurities of a second conductivity type opposite to said first conductivity type into ~~each~~ a surface layer of said second ~~regions~~ region, and thereafter executing a first activation process to form first impurity diffusion ~~regions~~ region;

(d) forming first spacer ~~films~~ film on side ~~surfaces~~ surface of said first gate ~~electrodes~~ electrode;

(e) by using said first gate ~~electrodes~~ electrode and said first spacer ~~films~~ film as a mask, implanting impurities of said second conductivity type into ~~each~~ a surface layer of

said first ~~regions~~ region, and thereafter executing a second activation process to form a second impurity diffusion ~~regions~~ region;

(f) removing said first spacer ~~films~~ film; and

(g) by using said first gate ~~electrodes~~ electrode as a mask, implanting impurities of said second conductivity type into ~~each~~ a surface layer in said first ~~regions~~ region and thereafter executing a third activation process to form third impurity diffusion ~~regions~~ region, wherein said third activation process is executed so that the gradient of an impurity concentration distribution in a p-n junction formed by the third impurity diffusion ~~regions~~ region becomes steeper than the gradient of an impurity concentration distribution in a p-n junction formed by said first impurity diffusion ~~regions~~ region formed by said first activation process.

13. (Amended) A method of manufacturing a semiconductor device according to claim 10, wherein the ~~shortest~~ gate length ~~among~~ of said first gate ~~electrodes~~ electrode is shorter than the ~~shortest~~ gate length ~~among~~ of said second gate ~~electrodes~~ electrode.

14. (Amended) A method of manufacturing a semiconductor device~~, comprising the steps of:~~ according to claim 11, wherein said step (c) is performed after said steps (d) and (e)

~~(a) preparing a semiconductor substrate having first and second regions of a first conductivity type defined in a principal surface area of the semiconductor substrate;~~

~~(b) forming at least first gate electrodes in a partial area of said first region;~~

~~(c) forming first spacer films on side surfaces of said first gate electrodes;~~

~~(d) by using said first gate electrodes and first spacer films as a mask, implanting impurities of a second conductivity type opposite to said first conductivity type into surface layer of said first region, and thereafter executing first activation process to form first impurity diffusion regions;~~

~~(e) implanting impurities of the second conductivity type into surface layer of the second regions, and thereafter executing a second activation process to form second impurity diffusion regions;~~

~~(f) removing said first spacer films; and~~

~~(g) by using said first gate electrodes as a mask, implanting impurities of said second conductivity type into surface layer in said first regions and thereafter executing a third activation process to form third impurity diffusion regions, wherein said third activation process is executed so that the gradient of an impurity concentration distribution in a p-n junction formed by said third impurity diffusion regions becomes steeper than the gradient of an impurity concentration distribution in a p-n junction formed by said second impurity diffusion regions formed by said second activation process~~.

17. (Amended) A method of manufacturing a semiconductor device according to claim 14, wherein the ~~shortest~~ gate length ~~among~~ of said first gate ~~electrodes~~ electrode is shorter than the ~~shortest~~ gate length ~~among~~ of said second gate ~~electrodes~~ electrode.